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| ESA număr: Building IP Core |
| SPACEWIRE IP CORE  HARDWARE USER MANUAL |

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|  | **Name and Function** | **Date** | **Signature** |
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| --- | --- | --- |
| **Document type** | **Nb WBS** | **Keywords** |

DOCUMENT CHANGE LOG

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Issue / Revision** | **Date** | **Modification Nb** | **Modified pages** | **Observations** |
| 0/0 | 14/10/2017 |  |  | Creation |

PAGE ISSUE RECORD

Issue of this document comprises the following pages at the issue shown

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Page | Issue/  Rev. | Page | Issue/  Rev. | Page | Issue/  Rev. | Page | Issue/  Rev. | Page | Issue/  Rev. | Page | Issue/  Rev. |
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# SCOPE

The present document is written in the framework of the ESA nr..... Face parte din faza xxxx a contractului privind proiectarea ........Activitatea se referă la proiectarea unui nucleu IP care va fi integrat in SOC.

Acest document este Manualul utilizatorului hardware al miezului VHDL. Este destinat utilizatorilor care ar dori să folosească blocul VHDL. Aceasta explică următoarele elemente:

* structure of the UNIX directories containing the core and the testbench,
* adaptation of the core to other technologies,
* structure of the two testbenches used to verify the core,
* test plan of the testbenches,
* run of the simulation,
* synthesis of the core

# DOCUMENTS AND ACRONYMS

## APPLICABLE DOCUMENTS

## REFERENCE DOCUMENTS

## ACRONYMS

# DESIGN DESCRIPTION

## ACCOUNT STRUCTURE

## THE VHDL SOURCE DESCRIPTION

## CONFIGURATION OF THE SPICEWIRE BLOCK

### FIFO configuration

### Counter configuration

### Tx Clock configuration

## PORTING OF THE SPACEWIRE CORE TO DIFFERENT TECHNOLOGY

# SIMULATION PLAN

## INTRODUCTION

## TEST OF THE SPACEWIRE WITHOUT THE HOST INTERFACE

## TEST OF THE HOST INTERFACE

### Test sequences run during the test of the host interface

#### Introduction

#### TX AHB master interface test 1: nominal operation

#### RX AHB master interface test 1: area middle address= area end address

#### RX AHB master interface test 2: RX FIFO is full and RX FIFO dumping

#### RX AHB master interface test 3: area middle address

#### RX AHB master interface test 4: RX FIFO dumping

#### RX AHB master interface test 5: memory area swap

#### RX AHB master interface test 6: RX FIFO dumping

#### TX AHB master interface test 2: packet abortion

#### Test of Area1\_valid and Area2\_valid flags

#### TX AHB master interface test 3: new transfer after packet abortion

#### Test of the interrupts (IT)

#### Test of time code

#### TX AHB slave interface test 1: ERROR response

#### TX AHB master interface test 4

#### TX AHB master interface test 5

#### TX AHB master interface test 6

#### TX AHB master interface test 7

#### Test of LINK\_NOT\_ENABLED IT

#### TX AHB slave interface test 2: nominal operation

#### RX AHB master interface test 7

#### RX AHB master interface test 8

#### RX AHB master interface test 9

#### RX AHB master interface test 10

#### RX AHB master interface test 11

#### RX AHB master interface test 12

#### RX AHB master interface test 13

#### RX AHB master interface test 14

#### RX AHB master interface test 15

#### RX AHB master interface test 16

#### RX AHB master interface test 17

#### RX AHB master interface test 18: Area2\_valid flag clearing

#### RX AHB master interface test 19: Check the last part of the packet

#### TX AHB master interface test 8: the FSM reads a packet size = 0

#### Test 1 of the interface between the AHB FIFO and the TX FIFO

#### Test 2 of the interface between the AHB FIFO and the TX FIFO

#### Test of the TX FIFO flush when the link is disabled

#### Test 1 to increase the test coverage: test of the sw\_reg block

#### Test 2 to increase the test coverage: adds an EEP to the RX FIFO

#### Test of the initialization protocol to increase the test coverage

## SIMULATION DESCRIPTION

### Simulation without the host interface

### Simulation with the host interface

## SIMULATION REPORT

# XILINX SYNTHESIS

## SET-UP AND DEVICE

## COMPILATION AND MAPPING OPTIONS

## CONSTRAINTS

## RESULTS

## SYNTHESIS CONCLUSION

# XILINX PLACE AND ROUTE

## 6.1 PRESENTATION

## 6.2. CONSTRAINTS

## 6.3. RESULT

### 6.3.1. Device utilization summary

### 6.3.2. Constraint report

## 6.4. LAYOUT CONCLUSION

## 6.5. CAO TOOLS CONFIGURATION